IN THE SPECIFICATION

The Examiner stated that it is unclear as to whether the reference (510) on page 21, line 10 should be referencing (508) in Figure 5. Please amend the paragraph on page 21, line 8 – page 22, line 12 in the manner noted below. The amendment is believed to introduce no new matter.

After the first cut, critical paths are identified based on actual delay data from the known cuts and probabilistic estimates generated from the evaluation of other designs using traditional partitioning algorithms (508)~~(510)~~. The probabilistic estimates constitute the phase-local for that phase. For example, since the first cut may have placed the source design into left and right halves of the target device, HH delays from this cut are known. For those paths crossing the vertical boundary of the device, the total path delay will be a sum of the cuts and non-cuts. The cuts represent the delays using HH interconnects whereas the non-cuts represent the probabilistic estimate of future cuts. For example, for a given path comprising 7 connections and cut once by a partition, the estimated delay is the sum of the actual cuts (1 HH connection) and 6 non-cuts (6 times the phase local for this phase). This method permits a more accurate estimation of the delays to be expected from future cuts than provided by the mere use of a unit-delay. The combination of actual delays for cut connections and statistical estimates as applied to non-cut connections allows the tool to more accurately identify the critical paths. The source design is then partitioned with another cut using this revised critical path data (510), again attempting to minimize or avoid cuts across the newly identified critical paths. In one embodiment, a determination would follow as to whether the source design was fully placed (518), such as, for example, in the APEX 20K device described, whether the partitioning had proceeded through the 5 different phases or levels of hierarchy. Where the design had not yet been fully placed, the method would proceed to estimate the criticalities of connections (508), this time based on the new data, i.e. actual data from another cut or phase of partitioning and a new phase local for the upcoming phase. The new phase local would be a function of the probabilities applicable to the levels of cuts not yet made. These probabilities are determined by examining a sampling of electronic designs placed by conventional techniques and determining the percentage of cuts attributable to each level of cut. Following each partition phase, this loop, which includes estimating criticalities based on the new delay data (508) and partitioning to avoid or minimize cuts on critical paths so determined (510) is repeated until full placement of the source design.

5. The Examiner stated that (610) should read (620) on page 23, line 16. Please amend the paragraph on page 23, line 10 – page 24, line 5 in the manner noted below. The amendment is believed to introduce no new matter.

The statistical data for delays to be attributed to future cuts ensures a more accurate delay estimate than provided by estimates based only on the length of paths. As illustrated in the flowchart of Fig. 6, in order to generate the statistical data at least one electronic design is placed according to conventional partitioning techniques. The flow in this method commences with the receipt of the electronic design, which may be in the form of a netlist (610). The design is placed fully using conventional partitioning techniques (620)~~(610)~~ without reference to statistical estimates for future cuts. In other words, the critical path at each phase is determined by a combination of the actual cuts across sections, and a unit delay assigned to each of the uncut connections. Following full placement of the design, the connections are analyzed to determine the percentage of each type of cut in the fully placed design (630). A separate phase local is generated for each partition phase. For example, the probabilistic estimate or phase local for phase 3 would be determined by adding all connections cut by levels 3,4, and 5 partitions and determining a probabilistic estimated delay by multiplying the percentage of that particular level cut by the actual delays associated with that type of cut in the architecture. The process then proceeds to determine whether other designs in the sampling need to be analyzed (640). Once statistical data has been generated for all the designs in the sampling, the data is averaged over all designs (650). The conventional partitioning algorithm described is used to place all of the sample designs in an identical hardware target device. The averaged data comprises the statistical estimates to be used in block 508, shown in Fig. 5.